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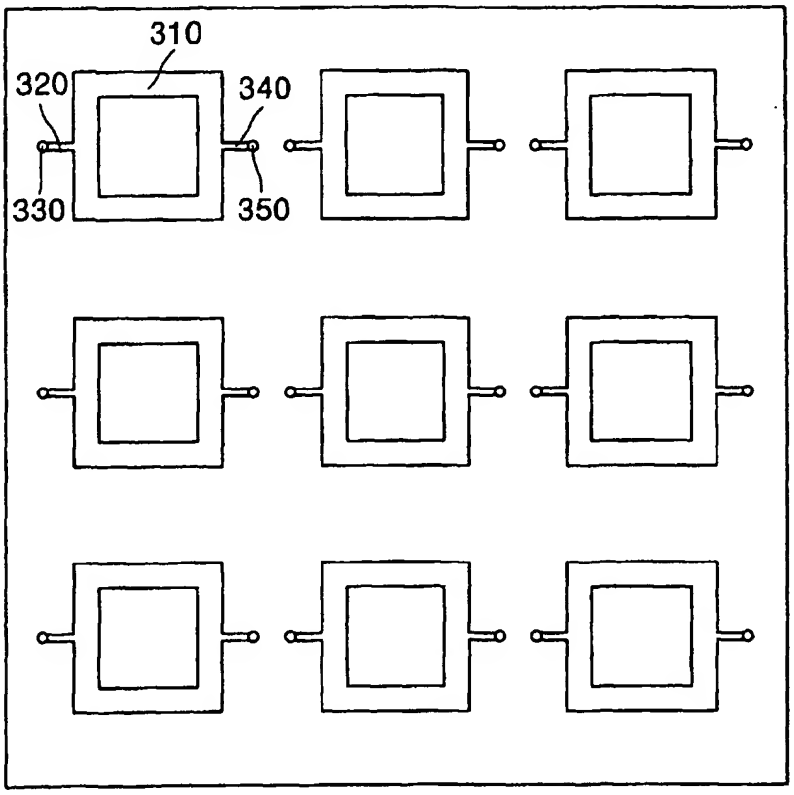
(54) Title: MOLD FOR USED IN MULTI FLIP-CHIP UNDERFILL ENCAPSULATION PROCESS



(57) Abstract: A mold for underfill encapsulation process of multi flip chip is disclosed. The mold has a multiplicity of cavities, in each of which each of said semiconductor chips is accommodated; a multiplicity of encapsulant inlets for guiding the injected encapsulant into said cavities; and a multiplicity of encapsulant outlets for exhausting the encapsulant and air in said cavities to the outside of said cavities. The mold for underfill encapsulation process of multi flip chip in accordance with the present invention is able to encapsulate numbers of flip chips at the same time, and thus it reduces the processing time required for encapsulation process and thereby remarkably improves the overall productivity.

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MOLD FOR USED IN MULTI FLIP-CHIP UNDERFILL ENCAPSULATION PROCESS

【 Technical Field 】

The present invention relates to a mold, and more particularly to a mold being used for an encapsulation process of multi flip chip, in which semiconductor chips are directly mounted on a substrate.

【 Background Art 】

Generally, a flip chip is constituted of directly mounting a semiconductor chip on a substrate, where the inputs/outputs of the semiconductor chip and the substrate are connected to each other by solder ball, conductive bonding agent, and so on. With this structure, a flip chip can minimize the connecting wires between a semiconductor chip and a substrate, and thereby achieve a high operation speed. However, a flip chip has a disadvantage that a bumper, which is a bonding-point, is occasionally being cracked during the manufacturing process due to the difference between the thermal expansion coefficients of a substrate and a semiconductor chip. Thus, in the manufacturing process of a flip chip, an underfill encapsulation process, locating a flip chip in a cavity of a mold and thereafter injecting encapsulant to fill the surroundings of the semiconductor chip as well as the space between the semiconductor chip and the substrate, is being required for providing a mechanical and electrical reinforcement to the flip chip.

A method of injecting encapsulant by using the capillarity phenomenon has been used for underfill encapsulation process in the prior art, however, it has problems that the price of encapsulant used therein is expensive and the processing speed is very slow.

To improve the speed of an encapsulation process, a couple of new methods for encapsulation process have been recently proposed such as an encapsulation method of using a vacuum, developed by M. K. Schwiebert, W. H. Leong and K. Banerji, and a compressed underfill encapsulation method developed by K. K. Wang and Se-Jin Hahn, the inventor of the present invention.

Compared with the prior art, the encapsulation method of using a vacuum mentioned above remarkably reduces the processing time required for injecting the encapsulant into the cavity of a mold, wherein a flip chip is located, however, the maximum driving power is limited to the atmospheric pressure. Consequently, the method of using a vacuum described above can be effectively applicable to an encapsulation process using low-viscosity encapsulant, however, it is not suitable for the process using high-viscosity encapsulant.

The compressed underfill encapsulation method mentioned above is a method of injecting the encapsulant with a high-pressure into the cavity of a mold, wherein a flip chip is located. It also remarkably reduces the processing time required for filling the cavity with the encapsulant, however, the encapsulant, remained in the mold after the injecting process, has to be washed-out before carrying out the next encapsulation process, and thus, it requires large amount of processing time for carrying out the process.

In addition, the distance between the chip and the side-wall of the cavity is arbitrarily set in a mold, used for the vacuum encapsulation process or the compressed underfill encapsulation process described above. And thus, as described in FIG. 1, it is very likely that voids are formed in the space between the bonding parts after the encapsulation process. In more detail, FIG. 1 is a view illustrating the encapsulation result of encapsulating a chip, whose long-directional and short-directional lengths are

10mm each, apart by about 0.1mm from a substrate, by using a mold in which the distance between the chip and the side-wall of the cavity is 0.8mm. It shows that a void is formed in the upper center portion.

【 Disclosure of Invention 】

It is the object of the present invention to provide a mold for underfill encapsulation process of multi flip chip that can effectively solve the problems of the prior art mentioned above.

In one aspect of the present invention, there is a mold for underfill encapsulation process of multi flip chip, wherein semiconductor chips are directly mounted on a substrate. The mold for underfill encapsulation process of multi flip chip, according to the one aspect of the present invention, comprises a multiplicity of cavities, open to the direction of facing said substrate, in each of which each of said semiconductor chips is accommodated during said encapsulation process; a multiplicity of encapsulant inlets, formed at one side of said cavities, for guiding the injected encapsulant into said cavities during said encapsulation process; and a multiplicity of encapsulant outlets, formed at the other side of said cavities, for exhausting the encapsulant and air in said cavities to the outside of said cavities during said encapsulation process. Wherein, the maximum allowable separation distance(b) between said semiconductor chip and the side-wall of said cavity is limited according to the long-directional distance(W) of said semiconductor chip, the short-directional distance(D) of said semiconductor chip, and the spacing(h) between the bottom surface of said semiconductor chip and said substrate.

In another aspect of the present invention, there is a mold for underfill encapsulation process of multi flip chip, wherein semiconductor chips are directly mounted on a substrate. The mold for underfill encapsulation process of multi flip chip,

according to the another aspect of the present invention, comprises a cavity, open to the direction of facing said substrate, in which said semiconductor chips are accommodated during said encapsulation process; an encapsulant inlet, formed at one side of said cavity, for guiding the injected encapsulant into said cavity during said encapsulation process; and an encapsulant outlet, formed at the other side of said cavity, for exhausting the encapsulant and air in said cavity to the outside of said cavity during said encapsulation process. Wherein, the maximum allowable separation distance(b) between the semiconductor chip located at the side of said cavity, among said semiconductor chips accommodated in said cavity, and the side-wall of said cavity is limited according to the long-directional distance(W) of said semiconductor chip, the short-directional distance(D) of said semiconductor chip, and the spacing(h) between the bottom surface of said semiconductor chip and said substrate.

【 Brief Description of Drawings 】

The foregoing and further features and advantages of the invention will become more apparent from the following description and the accompanying drawings, in which the same reference numerals indicate the same or corresponding parts:

FIG. 1 is a view illustrating the encapsulation result of encapsulating a flip chip in prior art.

FIG. 2a is a bottom view of a mold for underfill encapsulation process of multi flip chip, in accordance with the first embodiment of the present invention.

FIG. 2b is a sectional view illustrating the structure of the mold described in FIG. 2a.

FIG. 3a and FIG. 3b are views for explaining the maximum allowable separation distance between said semiconductor chip and the side-wall of said cavity, in

accordance with the first embodiment of the present invention.

FIG. 4 is a view illustrating the encapsulation result of encapsulating a flip chip, in accordance with the first embodiment of the present invention.

FIG. 5a is a bottom view of a mold for underfill encapsulation process of multi flip chip, in accordance with the second embodiment of the present invention.

FIG. 5b is a sectional view illustrating the structure of the mold described in FIG. 5a.

FIG. 6a is a bottom view of a mold for underfill encapsulation process of multi flip chip, in accordance with the third embodiment of the present invention.

FIG. 6b is a sectional view illustrating the structure of the mold described in FIG. 6a.

FIG. 7a is a bottom view of a mold for underfill encapsulation process of multi flip chip, in accordance with the fourth embodiment of the present invention.

FIG. 7b is a sectional view illustrating the structure of the mold described in FIG. 7a.

FIG. 8a is a bottom view of a mold for underfill encapsulation process of multi flip chip, in accordance with the fifth embodiment of the present invention.

FIG. 8b is a sectional view illustrating the structure of the mold described in FIG. 8a.

FIG. 9a is a bottom view of a mold for underfill encapsulation process of multi flip chip, in accordance with the sixth embodiment of the present invention.

FIG. 9b is a sectional view illustrating the structure of the mold described in FIG. 9a.

FIG. 10a is a bottom view of a mold for underfill encapsulation process of multi flip chip, in accordance with the seventh embodiment of the present invention.

FIG. 10b is a sectional view illustrating the structure of the mold described in FIG. 10a.

【 Best Mode for Carrying Out the Invention 】

Hereinafter, referring to appended drawings(FIG. 2a ~ FIG. 10b), the structures of the embodiments of a mold for underfill encapsulation process of multi flip chip in accordance with the present invention are described in detail.

FIG. 2a is a bottom view of a mold for underfill encapsulation process of multi flip chip in accordance with the first embodiment of the present invention, and FIG. 2b is a sectional view illustrating the structure of the mold described in FIG. 2a. Referring to FIG. 2a and FIG. 2b, a mold in accordance with the first embodiment of the present invention comprises numbers of cavities(310), encapsulant inlets(320), injection holes(330), encapsulant outlets(340), and exhaustion holes(350).

Numbers of cavities(310) are formed at the bottom of a mold. Each cavity(310) is open toward the substrate(2) and has a size to be able to accommodate one semiconductor chip(1) mounted on the substrate(2) during the encapsulation process. A cavity(310) is formed to be bigger than a semiconductor chip(1). However, for preventing the void formation in the space between the bonding parts, i. e., the space between the semiconductor chip(1) and the substrate(2), during the encapsulation process, it is formed to limit the surrounding areas of the semiconductor chip(1) within a specific value according to the size of the semiconductor chip(1). Explaining more detail with referring to FIG. 3a and FIG. 3b, the maximum allowable width(b) of the surrounding area, in other words the maximum allowable separation distance(b) from the side-wall(312) of the cavity(310) to the side surface of the semiconductor chip(1), is defined by the following equation[Eqn. (1)].

[Equation 1]

$$b^4 - \frac{(W+D)^2 h^2}{0.1542WD} b^2 - \frac{(W+D)h^3}{0.1542} = 0.0 \ .$$

In the equation[Eqn. (1)], W is the long-directional length of the semiconductor chip(1) located in the cavity(310), D is the short-directional length of the semiconductor chip(1), and h is the spacing between the bottom surface of the semiconductor chip(1) and the substrate(2). And the value, 0.1542, is an experimentally obtained constant. For example, in case that the long-directional length(W) and the short-directional length(D) of a semiconductor chip(1) are 10mm each and the spacing(h) between the bottom surface of the semiconductor chip(1) and the substrate(2) is 0.1mm, the maximum allowable separation distance(b) is about 0.71mm.

In the experiments of encapsulation process of a semiconductor chip(1), having the size described above, using a mold constituted with the maximum allowable separation distance(b), obtained by the equation described above, being applied thereto, no void is formed in the space between the semiconductor chip(1) and the substrate(2) as shown in FIG. 4a and FIG. 4b. Here, FIG. 4a shows the case that the width of the surrounding area(i. e., separation distance) is about 0.6mm, and FIG. 4b shows the case that the width of the surrounding area is about 0.7mm.

In addition, the cavity(310) is constituted to have a sufficient height with which the mold is separated from the upper surface of a semiconductor chip(1), during the encapsulation process, with a certain distance. And thus, even when numbers of flip chips having different heights are being encapsulated simultaneously, it prevents that comparatively high semiconductor chips are being damaged by being contacted with the

mold. Preferably, the cavity(310) is constituted that the spacing between the mold surface(314) and the semiconductor chip(1) is smaller than the spacing(h) between the bottom surface of the semiconductor chip(1) and the upper surface of the substrate(2).

An encapsulant inlet(320) is formed at one side of each cavity(310) to be stream-linked to the cavity(310) and guides the injected encapsulant to the inside of the cavity(310) during the encapsulation process.

Each injection hole(330) is formed to the direction of mold thickness and stream-linked to each encapsulant inlet(320). Through the injection hole(330), an encapsulant injecting plunger(not described in the figure) of the encapsulation apparatus injects encapsulant into the cavity(310) by compression during the encapsulation process.

Each encapsulant outlet(340) is formed at the other side of each cavity(310) to be stream-linked to the cavity(310) and exhausts the surplus encapsulant passing through the cavity(310) and the air inside the cavity(310) during the encapsulation process.

Each exhaustion hole(350) is formed to the direction of mold thickness, i. e. parallel to the injection hole(330), and stream-linked to each encapsulant outlet(340). The exhaustion hole(350) guides the encapsulant and air being exhausted through the encapsulant outlet(340) to the outside.

In the case of carrying out an underfill encapsulation process of a flip chip with using a mold of the present invention as described above, when an injecting plunger of the encapsulation apparatus is being positioned at an injection hole(330) and compresses the encapsulant, the compressed encapsulant is injected into a cavity(310) through an inlet(320) to be filled in the space between a semiconductor chip(1) and the substrate(2) as well as to be surrounded around the semiconductor chip(1). At this time,

the surplus encapsulant passing through the cavity(310) and the air inside the cavity(310) are coming out through an outlet(340) and exhausted through an exhaustion hole(350) to the outside.

As described above, a mold in accordance with the present invention can encapsulate numbers of flip chips at the same time with being equipped with numbers of cavities(310), each of which has an optimal size according to the size of a semiconductor chip(1) to be encapsulated therein. And thus, it can prevent the void formation in the space between the semiconductor chip(1) and the substrate(2) and the damage of the semiconductor chip(1) due to the direct contact with the mold.

A mold for underfill encapsulation process of multi flip chip in accordance with the present invention is not limited to the first embodiment described above, and it can also be embodied to have various modified structures that will be describes hereinafter.

Referring to FIG. 5a ~ FIG. 10b, the second ~ the seventh embodiments of a mold for underfill encapsulation process of multi flip chip in accordance with the present invention are now being described in detail. For a brief description, the detail description is mainly fulfilled on the parts different from previous embodiments, and the explanation on identical(or very similar) parts is omitted.

FIG. 5a is a bottom view of a mold for underfill encapsulation process of multi flip chip in accordance with the second embodiment of the present invention, and FIG. 5b is a sectional view illustrating the structure of the mold described in FIG. 5a. Referring to FIG. 5a and FIG. 5b, a mold in accordance with the second embodiment of the present invention comprises numbers of cavities(610), encapsulant inlets(620), injection holes(630), encapsulant outlets(640), exhaustion holes(650), and elastic bumpers(660).

The cavities(610), encapsulant inlets(620), injection holes(630), encapsulant

outlets(640) and exhaustion holes(650) are formed to be identical to those of the first embodiment and do the same function, and thus detail description on these elements will be omitted. Here, the maximum allowable width of the surrounding area around the semiconductor chip(1) located in the cavity(610) is also limited to the value calculated by the equation[Eqn. (1)] described in the first embodiment.

Each elastic bumper(660) is mounted at the upper surface of each cavity(610) facing a semiconductor chip(1) or the bottom surface of the mold facing the upper surface of the substrate(2), and thus it directly contacts with the upper surface of a semiconductor chip(1) or the upper surface of the substrate(2) during the encapsulation process. With this structure of equipping elastic bumpers(660), even when numbers of flip chips having different heights are being encapsulated simultaneously, it can prevent that the semiconductor chip(1) and the substrate(2) are being damaged by being contacted with the mold.

FIG. 6a is a bottom view of a mold for underfill encapsulation process of multi flip chip in accordance with the third embodiment of the present invention, and FIG. 6b is a sectional view illustrating the structure of the mold described in FIG. 6a. Referring to FIG. 6a and FIG. 6b, a mold in accordance with the third embodiment of the present invention comprises numbers of cavities(710), numbers of encapsulant inlets(720), a common injection hole(730), numbers of encapsulant outlets(740), numbers of exhaustion holes(750), and numbers of runners(760).

The cavities(710), encapsulant inlets(720) and encapsulant outlets(740) are formed to be identical to those of the first embodiment and do the same function, and thus detail description on these elements will be omitted. Here, the maximum allowable width of the surrounding area around the semiconductor chip(1) located in the cavity(710) is also limited to the value calculated by the equation[Eqn. (1)] described in

the first embodiment.

The common injection hole(730) is formed to be stream-linked to the encapsulant inlets(720), formed at one side of a certain number of cavities(710) located at one side of the mold, to inject the encapsulant simultaneously to the cavities(710) located at one side of the mold during the encapsulation process.

Each exhaustion hole(750) is stream-linked to each of the encapsulant outlets(740), formed at the other side of a certain number of cavities(710) located at the other side of the mold, to guide the encapsulant and air exhausted from the cavities(710) located at the other side of the mold to the outside during the encapsulation process.

Each runner(760) is stream-linked to an encapsulant outlet(740) of a cavity(710) and an encapsulant inlet(720) of the adjacent cavity(710) to guide the encapsulant and air exhausted through the encapsulant outlet(740) to the encapsulant inlet(720) connected thereto. In other words, adjacent cavities(710) are stream-linked to each other by runners(760). In this case, the encapsulant inlets(720) and the encapsulant outlets(740) of the cavities are formed to be the parts of the runners(760).

In an encapsulation process using a mold in accordance with the third embodiment of the present invention as described above, if the encapsulant is being injected into the cavities(710) located at one side of the mold through the common injection hole(730), surplus encapsulant and the inside air of the cavities(710) are provided to the adjacent cavities(710) through runners(760). In sequence, the encapsulant and air, provided to the adjacent cavities(710), are eventually provided to the cavities(710) located at the other side of the mold through the runners(760), and thereafter exhausted through the encapsulant outlets(740) of the cavities(710) located at the other side of the mold to the exhaustion holes(750). With this structure of reducing the numbers of injection holes(730) and exhaustion holes(750), the manufacturing

process of a mold becomes easier.

FIG. 7a is a bottom view of a mold for underfill encapsulation process of multi flip chip in accordance with the fourth embodiment of the present invention, and FIG. 7b is a sectional view illustrating the structure of the mold described in FIG. 7a. Referring to FIG. 7a and FIG. 7b, a mold in accordance with the fourth embodiment of the present invention comprises numbers of cavities(810), numbers of encapsulant inlets(820), a common injection hole(830), numbers of encapsulant outlets(840), numbers of exhaustion holes(850), numbers of runners(860), and numbers of elastic bumpers(870).

The cavities(810), encapsulant inlets(820), common injection hole(830), encapsulant outlets(840), exhaustion holes(850) and runners(860) are formed to be identical to those of the third embodiment and do the same function, and thus detail description on these elements will be omitted. Here, the maximum allowable width of the surrounding area around the semiconductor chip(1) located in the cavity(810) is also limited to the value calculated by the equation[Eqn. (1)] described in the first embodiment. And, the encapsulant inlets(820) and outlets(840) of adjacent cavities(810) are formed to be the parts of the runners(860).

Each elastic bumper(870) is mounted at the upper surface of each cavity(810) facing a semiconductor chip(1) or the bottom surface of the mold facing the upper surface of the substrate(2), and thus it directly contacts with the upper surface of a semiconductor chip(1) or the upper surface of the substrate(2) during the encapsulation process.

The function and effect of a mold for underfill encapsulation process of multi flip chip in accordance with the fourth embodiment of the present invention are similar to those of the mold in accordance with the third embodiment described before. In

addition, a mold in accordance with the fourth embodiment described above further comprises the elastic bumpers(870) so that it can prevent that the semiconductor chip(1) and the substrate(2) are being damaged by being directly contacted with the mold during the encapsulation process.

FIG. 8a is a bottom view of a mold for underfill encapsulation process of multi flip chip in accordance with the fifth embodiment of the present invention, and FIG. 8b is a sectional view illustrating the structure of the mold described in FIG. 8a. Referring to FIG. 8a and FIG. 8b, a mold in accordance with the fifth embodiment of the present invention comprises numbers of cavities(910), numbers of encapsulant inlets(920), a common injection hole(930), numbers of encapsulant outlets(940), and numbers of runners(950).

The cavities(910), encapsulant inlets(920), common injection hole(930) and runners(950) are formed to be identical to those of the third embodiment and do the same function, and thus detail description on these elements will be omitted. Here, the maximum allowable width of the surrounding area around the semiconductor chip(1) located in the cavity(910) is also limited to the value calculated by the equation[Eqn. (1)] described in the first embodiment. And, the encapsulant inlets(920) and outlets(940) of adjacent cavities(910) are formed to be the parts of the runners(950).

Among the encapsulant outlets(940), the outlets(940) formed at the cavities(910) located at the other side of the mold are constituted to be extended to the outside of the mold. With this structure, the outlets(940) of the cavities(910) located at the other side of the mold guide the encapsulant and air exhausted from the cavities(910) directly to the outside. And thus, a mold in accordance with the fifth embodiment of the present invention does not need the exhaustion holes that are required for the molds in accordance with the first ~ the fourth embodiments. Besides, since the outlets(940) are

formed to be parallel to the upper and lower surface of a mold, an external device such as an external vacuum pump(not described in the figure), for vacuuming out the surplus encapsulant and air, can be easily connected thereto.

The molds for underfill encapsulation process of multi flip chip in accordance with the first ~ the fifth embodiments of the present invention are figured and described in that each cavity is accommodating only one semiconductor chip(1) therein, however, the present invention is not limited to the structure described above and the cavity can also be designed to accommodate numbers of semiconductor chips(1) in other embodiments of the present invention.

FIG. 9a is a bottom view of a mold for underfill encapsulation process of multi flip chip in accordance with the sixth embodiment of the present invention, and FIG. 9b is a sectional view illustrating the structure of the mold described in FIG. 9a. Referring to FIG. 9a and FIG. 9b, a mold in accordance with the sixth embodiment of the present invention comprises a cavity(1010), an encapsulant inlet(1020), an injection hole(1030), an encapsulant outlet(1040), and an exhaustion hole(1050).

The cavity(1010) is formed to be the size able to simultaneously accommodate numbers of semiconductor chips(1) mounted on the substrate(2). And, the maximum allowable widths of the surrounding areas around the semiconductor chips(1) located at the sides of the cavity(1010) are limited to the values calculated by the equation[Eqn. (1)] described in the first embodiment.

The encapsulant inlet(1020), the injection hole(1030), the encapsulant outlet(1040) and the exhaustion hole(1050) are formed to be identical to those of the first embodiment and do the same function, and thus detail description on these elements will be omitted.

As described above, a mold in accordance with the sixth embodiment of the

present invention is able to carry out an encapsulation process of numbers of semiconductor chips(1) with much simpler structure than those of the first ~ the fifth embodiments.

FIG. 10a is a bottom view of a mold for underfill encapsulation process of multi flip chip in accordance with the seventh embodiment of the present invention, and FIG. 10b is a sectional view illustrating the structure of the mold described in FIG. 10a. Referring to FIG. 10a and FIG. 10b, a mold in accordance with the seventh embodiment of the present invention comprises a cavity(1110), an encapsulant inlet(1120), an injection hole(1130), an encapsulant outlet(1140), an exhaustion hole(1150), and numbers of elastic bumpers(1160).

The cavity(1110), the encapsulant inlet(1120), the injection hole(1130), the encapsulant outlet(1140) and the exhaustion hole(1150) are formed to be identical to those of the sixth embodiment and do the same function, and thus detail description on these elements will be omitted. And, just like in the sixth embodiment, the maximum allowable widths of the surrounding areas around the semiconductor chips(1) located at the sides of the cavity(1110) are limited to the values calculated by the equation[Eqn. (1)] described in the first embodiment.

Each elastic bumper(1160) is mounted at the upper surface of the cavity(1110) facing each semiconductor chip(1) or the bottom surface of the mold facing the upper surface of the substrate(2), and thus it directly contacts with the upper surface of the semiconductor chip(1) or the upper surface of the substrate(2) to prevent the damage of the semiconductor chip(1) and/or the substrate(2) possibly occurred due to the direct contact with the mold during the encapsulation process. While this invention has been particularly shown and described with reference to the first through the third embodiments thereof, it will be understood by those skilled in the art that various

changes and equivalents may be made without departing from the spirit and scope of the invention. Therefore, it is intended that the invention not be limited to the particular embodiment disclosed as the best mode contemplated for carrying out this invention, but that the invention will include all embodiments within the scope of the appended claims.

【 Industrial Applicability 】

As mentioned thereinbefore, a mold for underfill encapsulation process of multi flip chip in accordance with the present invention is able to encapsulate numbers of flip chips at the same time, and thus it reduces the processing time required for encapsulation process and thereby remarkably improves the overall productivity.

In addition, a mold in accordance with the present invention is equipped with cavities(310, 610, 710, 810, 910) –or, a cavity(1010, 1110)– having the size with which the void formation and the damage of the semiconductor chip(1) due to direct contact can be prevented during the encapsulation process, and thus it can remarkably reduce the defective fraction occurred in the encapsulation process.

What is claimed is:

1. A mold for underfill encapsulation process of multi flip chip, wherein semiconductor chips are directly mounted on a substrate, comprising:

a multiplicity of cavities, open to the direction of facing said substrate, in each of which each of said semiconductor chips is accommodated during said encapsulation process;

a multiplicity of encapsulant inlets, formed at one side of said cavities, for guiding the injected encapsulant into said cavities during said encapsulation process; and

a multiplicity of encapsulant outlets, formed at the other side of said cavities, for exhausting the encapsulant and air in said cavities to the outside of said cavities during said encapsulation process,

wherein the maximum allowable separation distance(b) between said semiconductor chip and the side-wall of said cavity is limited according to the long-directional distance(W) of said semiconductor chip, the short-directional distance(D) of said semiconductor chip, and the spacing(h) between the bottom surface of said semiconductor chip and said substrate.

2. A mold for underfill encapsulation process of multi flip chip in accordance with claim 1, further comprising:

a certain number of runners, formed to stream-link said inlets and outlets of adjacent cavities, to guide the encapsulant and air exhausted from said outlets to the inlets linked to said outlets.

3. A mold for underfill encapsulation process of multi flip chip in accordance with claim 2, further comprising:

at least one common injection hole, formed to be stream-linked to a certain number of inlets among said numbers of inlets, to inject the encapsulant therethrough into said certain number of inlets during said encapsulation process.

4. A mold for underfill encapsulation process of multi flip chip in accordance with claim 1, further comprising:

a multiplicity of injection holes, formed to be stream-linked to said inlets respectively, for injecting the encapsulant therethrough during said encapsulation process; and

a multiplicity of exhaustion holes, formed to be stream-linked to said outlets respectively, for guiding the encapsulant and air exhausted through said outlets to the outside.

5. A mold for underfill encapsulation process of multi flip chip n accordance with claims 1, 2, 3 or 4, wherein said maximum allowable separation distance(b) is determined to be the value obtained by the following equation:

$$b^4 - \frac{(W+D)^2 h^2}{0.1542WD} b^2 - \frac{(W+D)h^3}{0.1542} = 0 .$$

6. A mold for underfill encapsulation process of multi flip chip n accordance with claim 5, further comprising:

at least one elastic bumper, mounted at the inside surface of said cavity facing said semiconductor chip or the bottom surface of said mold facing said substrate, to be contacted with said semiconductor chip or said substrate during said encapsulation

process.

7. A mold for underfill encapsulation process of multi flip chip n accordance with claim 5,

wherein said cavity has a height with which the inside surface of said cavity is separated from the upper surface of said semiconductor chip by a certain spacing smaller than said spacing(h) between the bottom surface of said semiconductor chip and the upper surface of said substrate.

8. A mold for underfill encapsulation process of multi flip chip, wherein semiconductor chips are directly mounted on a substrate, comprising:

a cavity, open to the direction of facing said substrate, in which said semiconductor chips are accommodated during said encapsulation process;

an encapsulant inlet, formed at one side of said cavity, for guiding the injected encapsulant into said cavity during said encapsulation process; and

an encapsulant outlet, formed at the other side of said cavity, for exhausting the encapsulant and air in said cavity to the outside of said cavity during said encapsulation process,

wherein the maximum allowable separation distance(b) between the semiconductor chip located at the side of said cavity, among said semiconductor chips accommodated in said cavity, and the side-wall of said cavity is limited according to the long-directional distance(W) of said semiconductor chip, the short-directional distance(D) of said semiconductor chip, and the spacing(h) between the bottom surface of said semiconductor chip and said substrate.

9. A mold for underfill encapsulation process of multi flip chip n accordance with claim **8**, further comprising:

at least one elastic bumper, mounted at the inside surface of said cavity facing said semiconductor chip or the bottom surface of said mold facing said substrate, to be contacted with said semiconductor chip or said substrate during said encapsulation process.

10. A mold for underfill encapsulation process of multi flip chip n accordance with claim **8**,

wherein said cavity has a height with which the inside surface of said cavity is separated from the upper surface of said semiconductor chip by a certain spacing smaller than said spacing(h) between the bottom surface of said semiconductor chip and the upper surface of said substrate.

11. A mold for underfill encapsulation process of multi flip chip n accordance with claims **8, 9** or **10**,

wherein said maximum allowable separation distance(b) is determined to be the value obtained by the following equation:

$$b^4 - \frac{(W+D)^2 h^2}{0.1542WD} b^2 - \frac{(W+D)h^3}{0.1542} = 0 \ .$$

FIGURE 1

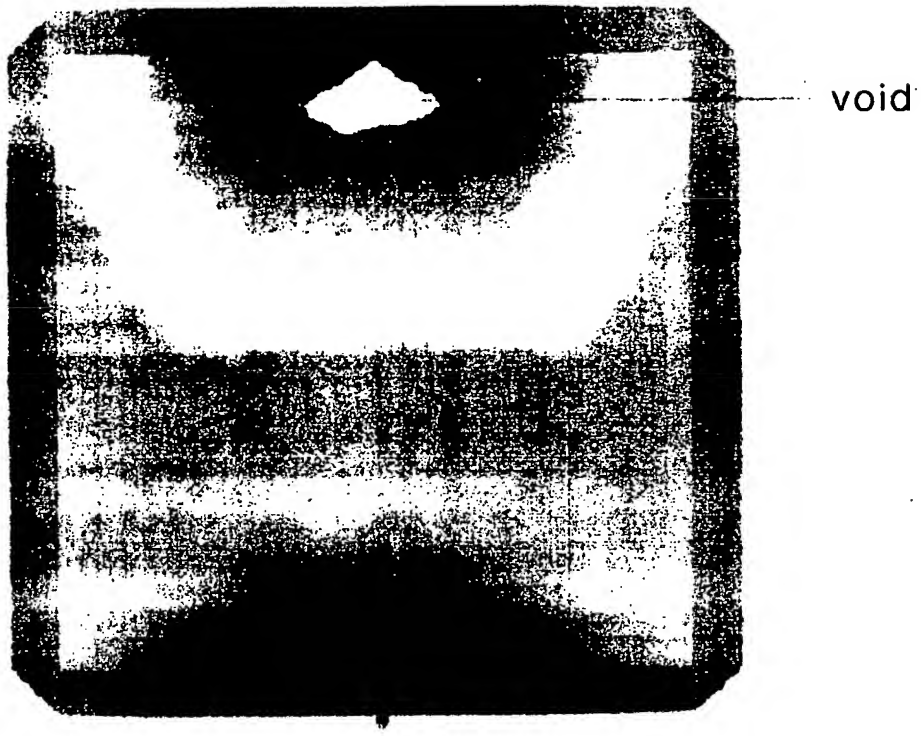


FIGURE 2a

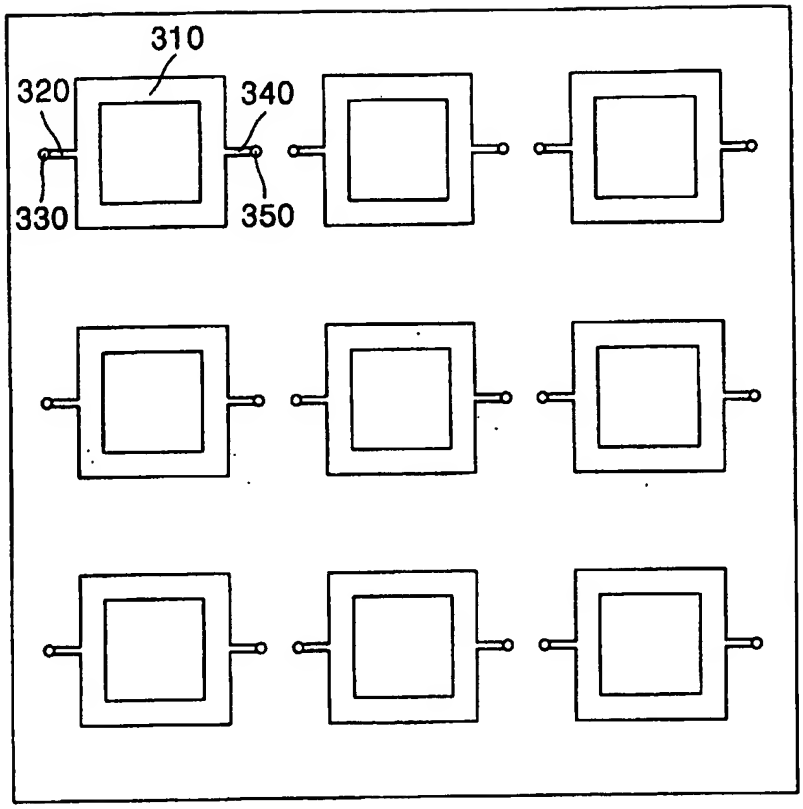


FIGURE 2b

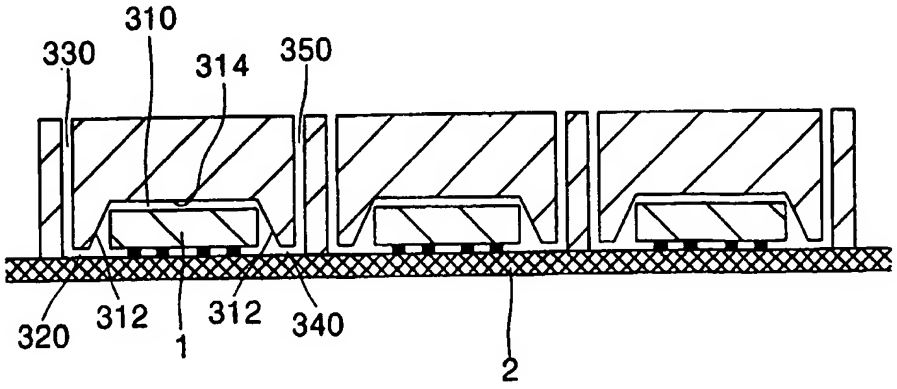


FIGURE 3a

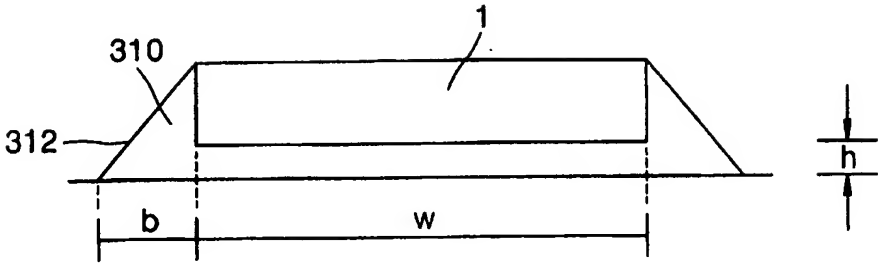


FIGURE 3b

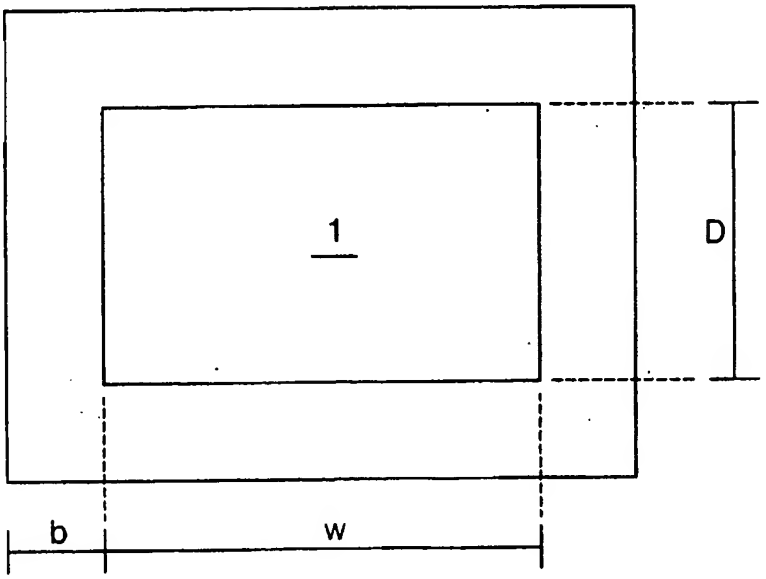


FIGURE 4a

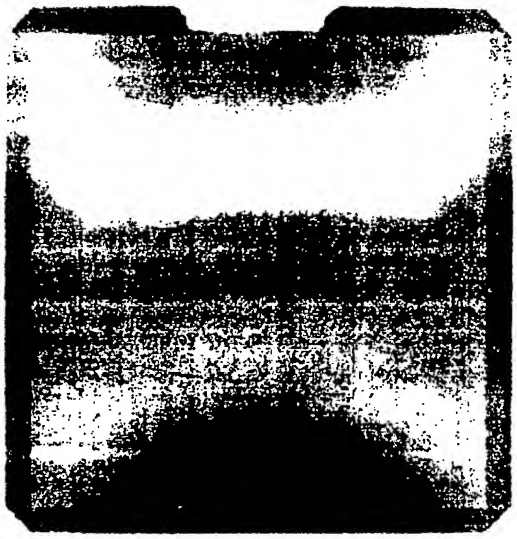


FIGURE 4a

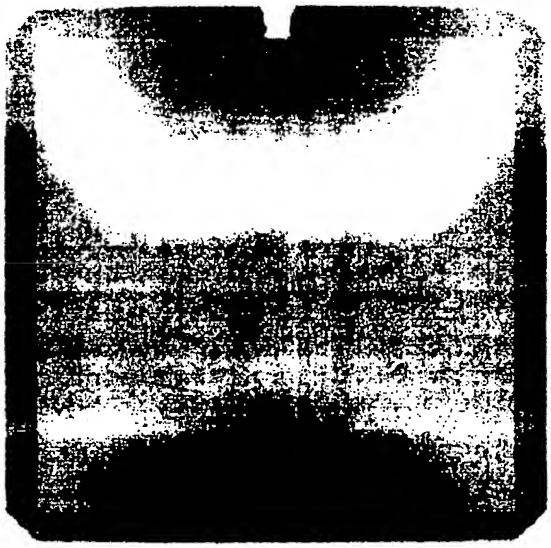


FIGURE 5a

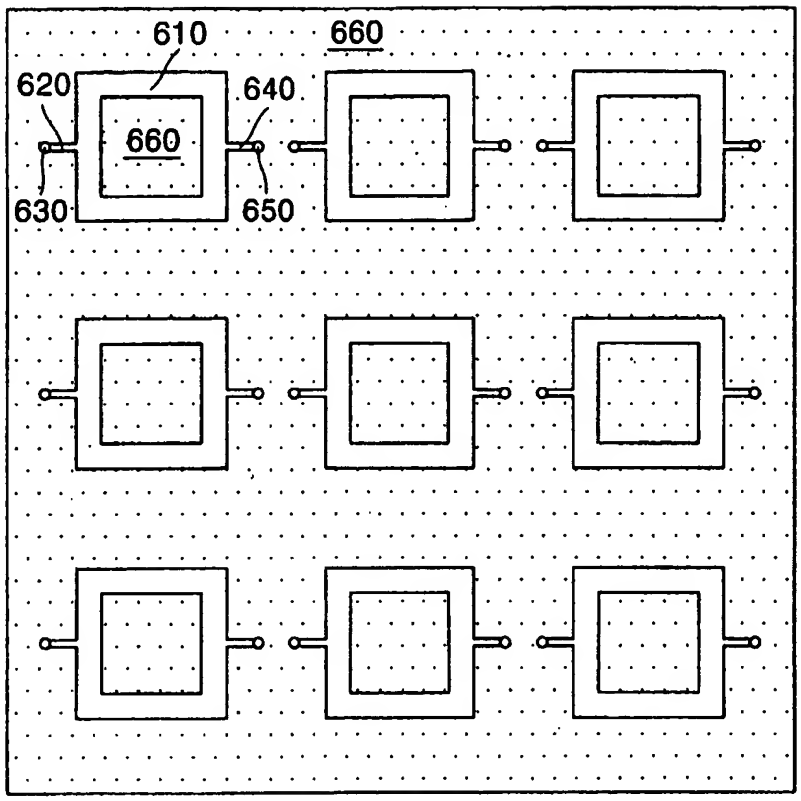


FIGURE 5b

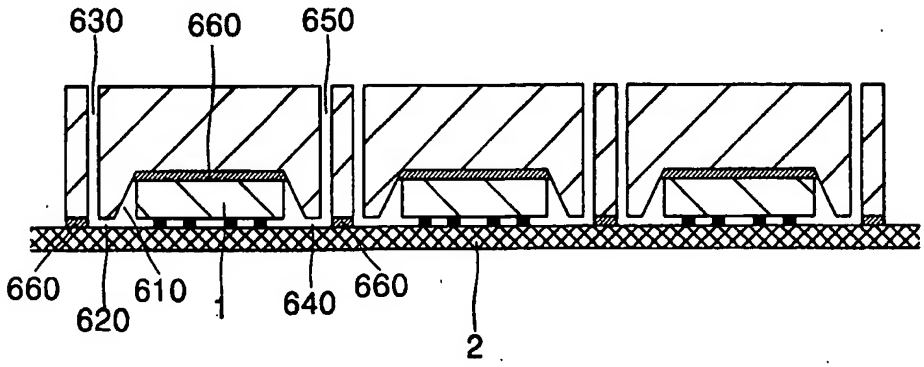


FIGURE 6a

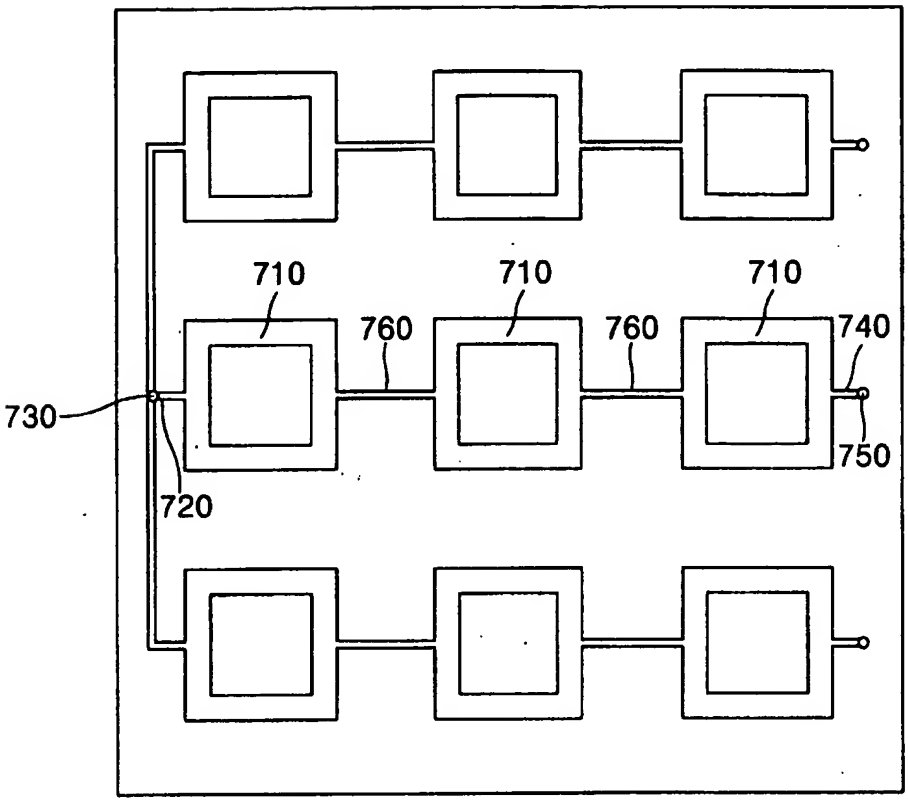


FIGURE 6b

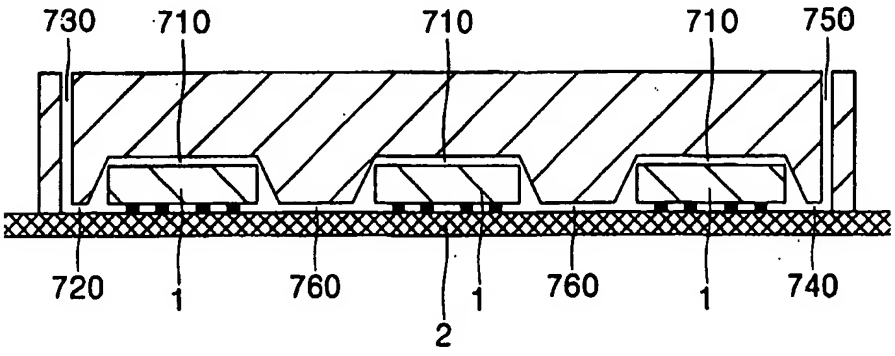


FIGURE 7a

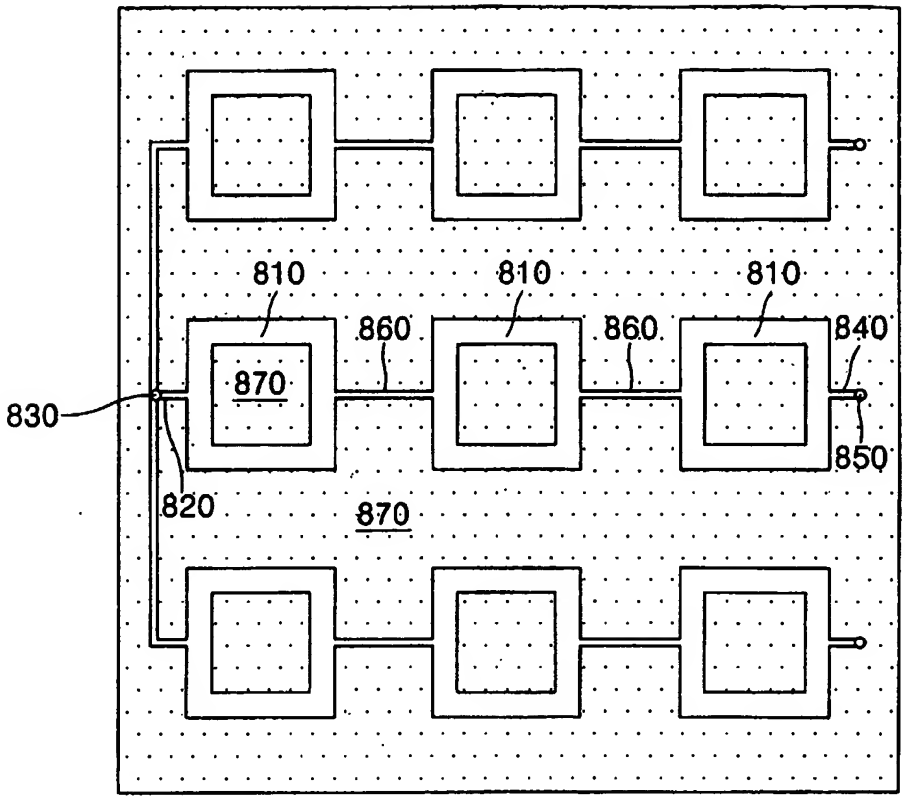


FIGURE 7b

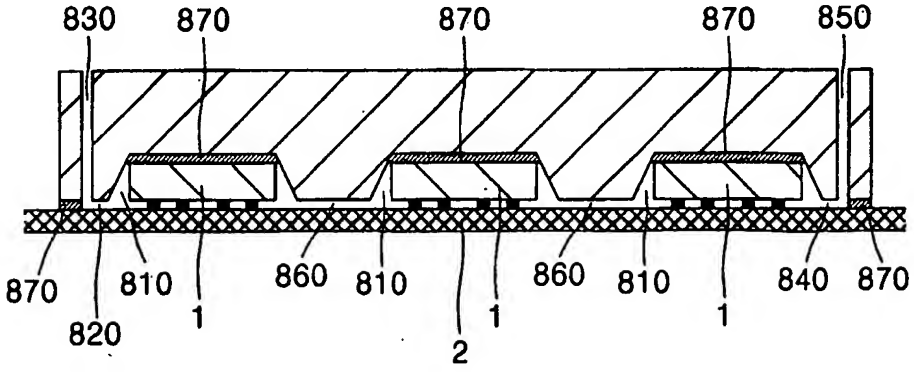


FIGURE 8a

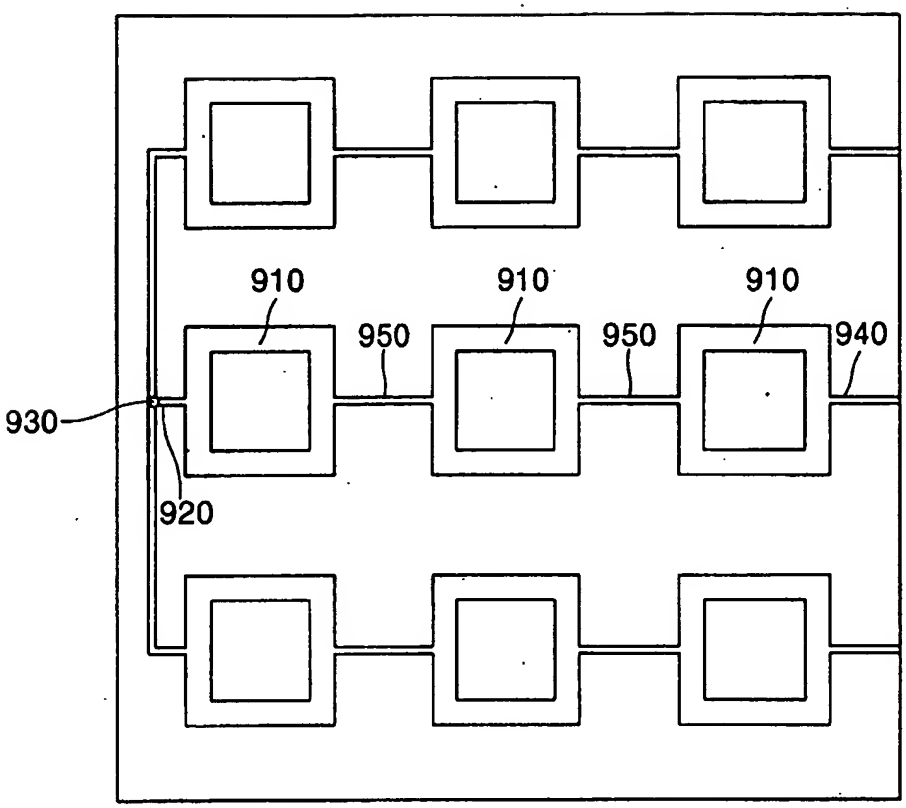


FIGURE 8b

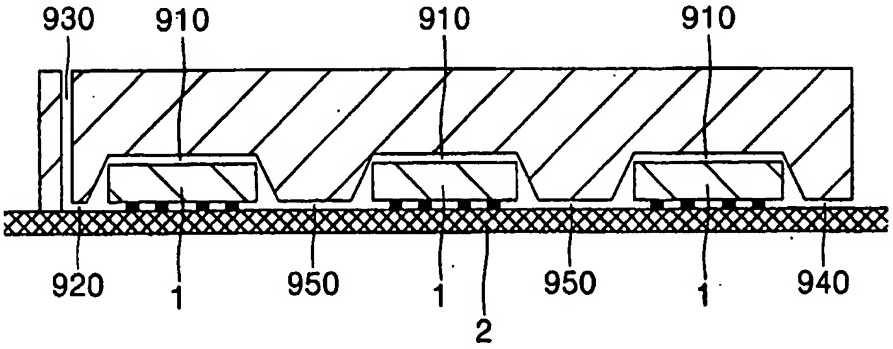


FIGURE 9

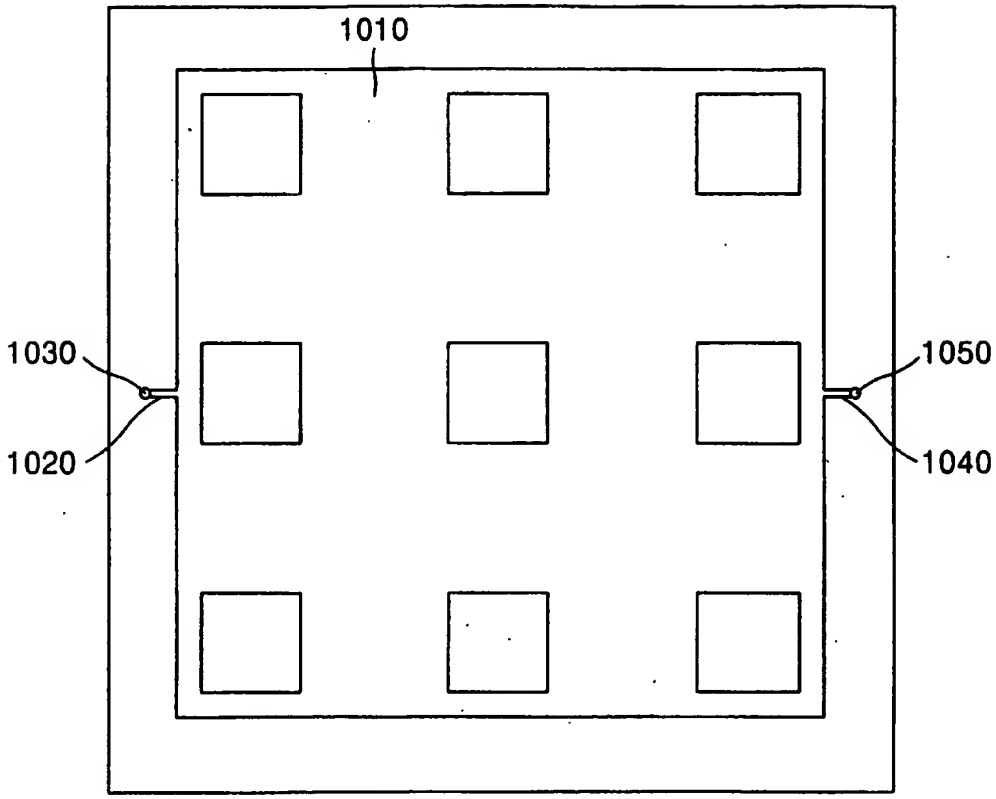


FIGURE 9b

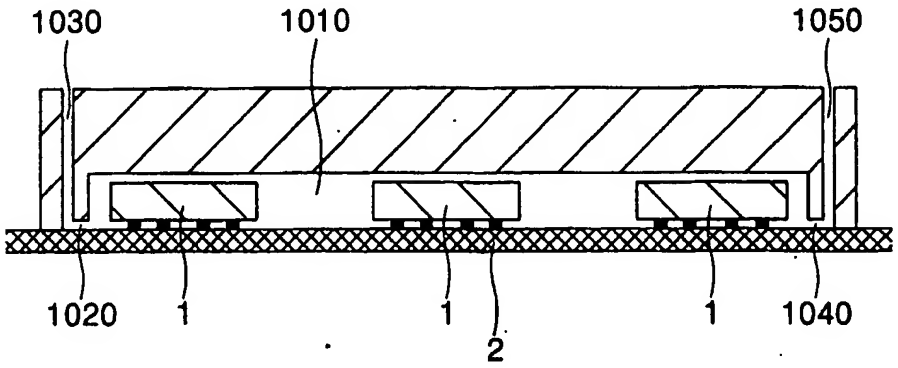


FIGURE 10a

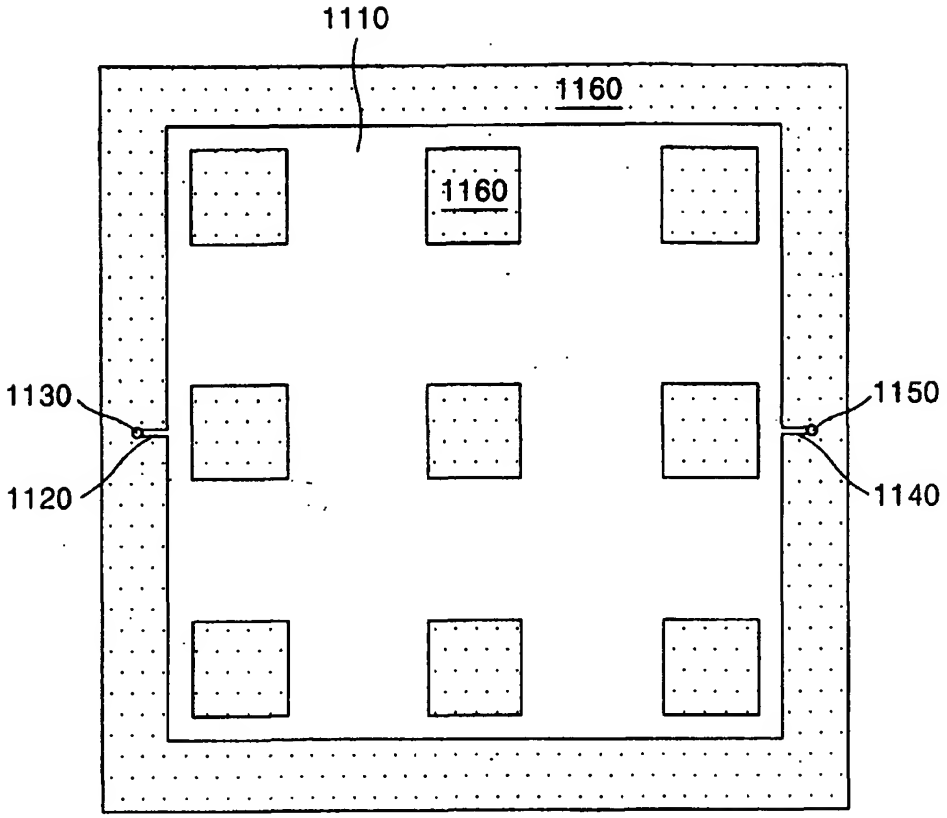
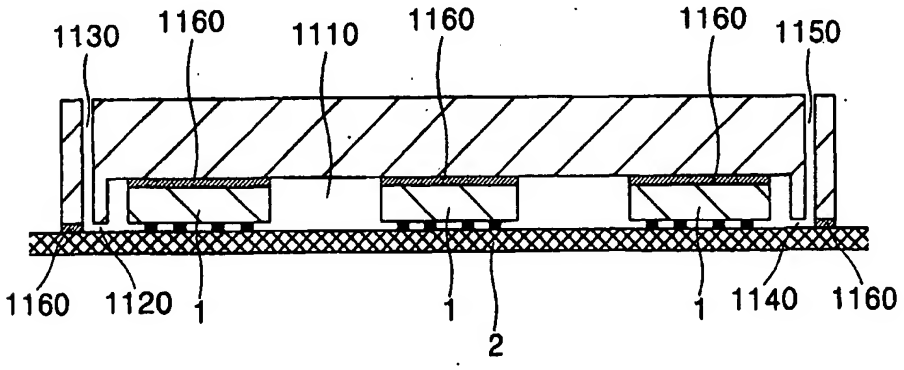


FIGURE 10b



INTERNATIONAL SEARCH REPORT

International application No.
PCT/KR02/02307

A. CLASSIFICATION OF SUBJECT MATTER

IPC7 H01L 21/56

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)

IPC7 H01L 21/60, B29C 45/02

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Korean Patents and applications for inventions since 1975.
Korean Utility models and application for Utility models since 1975.

Electronic data base consulted during the intertnational search (name of data base and, where practicable, search terms used)

KIPONET

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
A	US 5817545 A (Cornell Research Foundation, Inc.) 6 October 1998 * the whole document *	1 - 11
A	US 5998243 A (Toshiba K.K.) 7 December 1999 * the whole document *	1 - 11
A	JP 3-216309 A (Matsushita Electric IND. Co. Ltd.) 24 September 1991 * the whole document *	1 - 11

☐ Further documents are listed in the continuation of Box C.

☒ See patent family annex.

* Special categories of cited documents:

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"O" document referring to an oral disclosure, use, exhibition or other means

"P" document published prior to the international filing date but later than the priority date claimed

"T" later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention

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"Y" document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents,such combination being obvious to a person skilled in the art

"&" document member of the same patent family

Date of the actual completion of the international search	Date of mailing of the international search report
03 MARCH 2003 (03.03.2003)	06 MARCH 2003 (06.03.2003)

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Facsimile No. 82-42-472-7140

Authorized officer
SONG, Won Seon
Telephone No. 82-42-481-5735

INTERNATIONAL SEARCH REPORT

Information on patent family members

International application No.
PCT/KR02/02307

Patent document cited in search report	Publication date	Patent family member(s)	Publication date
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		WO 9727624 A	31.07.97
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		TW 393745 B	11.06.00
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